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EXAMINER	
BRADLEY, MATTHEW A	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 05/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,510	CHIU, KENNETH Y.	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Applicant's arguments, see Amendment After Final, filed 13 April 2006, with respect to the rejection(s) of claim(s) 1-24 under Khanna et al (U.S. 6,539,455) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Arimilli et al (U.S. 6,192,458).

As this Office action is being issued in response to amendments to the claims made 18 November 2005, this action has accordingly been made **FINAL**.

Claim Status

Claims 1-26 remain pending and are ready for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims **1-26** are rejected under 35 U.S.C. 102(a) and 35 U.S.C. 102(e) as being anticipated by Arimilli et al (U.S. 6,192,458) hereinafter referred to as Arimilli.

As per independent claim **1**, Arimilli teach,

- receiving a transfer request which corresponds to a block of data, wherein said block comprises a plurality of sub-blocks, said transfer request comprising an address and a mask which indicates which of said sub-blocks are required as part of the request; (Column 1 lines 16-54). *The Examiner notes that the 'block of data' as instantly claimed is taught by Arimilli as a "line in a cache", the 'plurality of sub-blocks' is taught by Arimilli as "particular bytes within the cache line". The transfer request as instantly claimed that comprises an 'address' is taught by Arimilli as an "address tag" which specifies a cache line within the set of two cache lines, and the "intra cache line address" teaches the mask as it allows a particular byte to be selected from the cache line.*
- generating a different address for each of said sub-blocks in response to receiving the transfer request; (Column 1 lines 16-54) *The Examiner notes that the addresses are different to allow one to be selected over the other and vice versa.*
- detecting which of said sub-blocks are required as part of said transfer request; (Column 1 lines 16-54) *The Examiner notes that as mentioned supra, the "intra cache line address" allows detection of which 'sub-block', "particular byte", is required as part of the transfer request.*

- and utilizing only those generated addresses which correspond to the sub-blocks which are required (Column 1 lines 16-54). *The Examiner notes that the "particular byte" is selected which teaches 'utilizing only those generated addresses ... to the sub-blocks which are required.'*

As per dependent claim **2**, Arimilli teach, wherein detecting which of said sub-blocks are required comprises examining said mask (Column 1 lines 16-54). *The Examiner notes that the "intra-cache line address", mask as shown supra, allows a particular byte to be selected, thus in order for the byte to be selected, the "intra-cache line address" must be examined.*

As per dependent claim **3**, Arimilli teach, wherein said mask comprises a separate bit for each of said sub-blocks, wherein a bit with a first value indicates a corresponding sub-block is required, and wherein a bit with a second value indicates a corresponding sub-block is not required (Column 1 lines 42-43 and 51-54). *The Examiner notes that the "intra-cache line address" as shown supra as the mask, allows a particular byte to be selected. The address itself is comprised of six bits, thus in order for the system to know which byte to select, the bits must indicate this. A particular byte being selected would require a particular bit to indicate this meaning the other bits indicate the other particular byte not being required.*

As per dependent claim **4**, Arimilli teach, wherein said request includes an address corresponding to said block, and wherein said transfer comprises transferring one of said sub-blocks at a time (Column 1 lines 16-54). *The Examiner notes that as shown supra, the "address tag" specifies a cache line 'block', and the "intra-cache line"*

specifies which 'sub-block' is to be transferred. One of the "particular bytes" are being selected and thus are transferred one at a time.

As per dependent claim **5**, Arimilli teach, wherein each of said addresses corresponding to said sub-blocks are generated concurrently (Column 1 lines 16-54).

As per dependent claim **6**, Arimilli teach, wherein said detecting comprises: detecting a first bit of said mask which has a first value, wherein said first bit corresponds to a first sub-block; and selecting a first address of said generated addresses which corresponds to the first sub-block (Column 1 lines 16-54). *The Examiner notes that as discussed supra, the "intra-cache line address" corresponds to a 'first sub-block' and is selected based on its occupancy in the cache line.*

As per dependent claim **7**, Arimilli teach, wherein said detecting further comprises: masking off said first bit of said mask, subsequent to utilizing said first address; detecting a second bit of said mask which has a first value, wherein said second bit corresponds to a second sub-block; and selecting a second address of said generated addresses which corresponds to the second sub-block (Column 1 lines 16-54). *The Examiner notes that as discussed supra, the "intra-cache line address" allows the selection of a particular byte. The system requiring a different particular byte then as discussed supra makes the request indicating the other particular byte.*

As per dependent claim **8**, Arimilli teach, determining a first number of said sub-blocks are required; and detecting transfer of all said required sub-blocks are complete, in response to detecting a number of sub-blocks equal to said first number have been transferred (Column1 lines 16-54). *The Examiner notes that as discussed supra, a*

particular byte is requested. Further, once the particular byte is selected, it is forwarded and thus the request is complete having transferred a single particular byte in response to the request for the particular byte.

As per independent claim **9**, the Examiner notes that in addition to the limitations as discussed supra with respect to independent claim 1, the instant claim further recites a first interface and a second interface embodied on a device (Column1 lines 16-54). *The Examiner notes that the cache as a whole receives the transfer request as discussed supra with respect to claim 1,thus teaching the first interface, and the individual pieces within the system comprise the second interface specifically pieces 302 and 312 as shown in Figure 3 as they break apart the transfer request to select the particular byte that is being requested.*

As per dependent claim **10**, Arimilli teach, wherein said second interface is further configured to detect which of said sub-blocks are required by examining said mask (Column 1 lines 16-54). *The Examiner notes that the "intra-cache line address", mask as shown supra, allows a particular byte to be selected, thus in order for the byte to be selected, the "intra-cache line address" must be examined.*

As per dependent claim **11**, Arimilli teach, wherein said mask comprises a separate bit for each of said sub-blocks, wherein a bit with a first value indicates said corresponding sub-block is required, and wherein a bit with a second value indicates said corresponding sub-block is not required (Column 1 lines 42-43 and 51-54). *The Examiner notes that the "intra-cache line address" as shown supra as the mask, allows a particular byte to be selected. The address itself is comprised of six bits, thus in order*

for the system to know which byte to select, the bits must indicate this. A particular byte being selected would require a particular bit to indicate this meaning the other bits indicate the other particular byte not being required.

As per dependent claim **12**, Arimilli teach, wherein said request includes an address corresponding to said block, and wherein said second interface is configured to initiate transfer of only one of said sub-blocks at a time (Column 1 lines 16-54). *The Examiner notes that as shown supra, the "address tag" specifies a cache line 'block', and the "intra-cache line" specifies which 'sub-block' is to be transferred. One of the "particular bytes" are being selected and thus are transferred one at a time.*

As per dependent claim **13**, Arimilli teach, wherein said second interface is configured to generate each of said addresses corresponding to said sub-blocks concurrently (Column 1 lines 16-54).

As per dependent claim **14**, Arimilli teach, wherein said second interface is configured to detect which of said sub-blocks are required by: detecting a first bit of said mask which has a first value, wherein said first bit corresponds to a first sub-block; and selecting a first address of said generated addresses which corresponds to the first sub-block (Column 1 lines 16-54). *The Examiner notes that as discussed supra, the "intra-cache line address" corresponds to a 'first sub-block' and is selected based on its occupancy in the cache line.*

As per dependent claim **15**, Arimilli teach, wherein said second interface is further configured to detect said required sub-blocks by: masking off said first bit of said mask, subsequent to utilizing said first address; detecting a second bit of said mask

which has a first value, wherein said second bit corresponds to a second sub-block; and selecting a second address of said generated addresses which corresponds to the second sub-block (Column 1 lines 16-54). *The Examiner notes that as discussed supra, the "intra-cache line address" allows the selection of a particular byte. The system requiring a different particular byte then as discussed supra makes the request indicating the other particular byte.*

As per dependent claim **16**, Arimilli teach, wherein said second interface is further configured to: determine a first number of said sub-blocks are required; and detect transfer of all said required sub-blocks are complete, in response to detecting a number of sub-blocks equal to said first number have been transferred Column1 lines 16-54). *The Examiner notes that as discussed supra, a particular byte is requested. Further, once the particular byte is selected, it is forwarded and thus the request is complete having transferred a single particular byte in response to the request for the particular byte.*

As per independent claim **17**, Arimilli teach,

- a control unit, wherein said control unit is configured to control access to a plurality of blocks of data, wherein each of said blocks of data comprise a plurality of sub-blocks, and wherein said control unit is not configured to convey a full block of said blocks of data at one time; (Figure 1 with respect to the control lines connecting the cache)
- a first interface coupled to said control unit, wherein said interface is configured to: (Figure 1 as shown in detail in Figure 3)

- receive a transfer request, wherein said request corresponds to a first block of said blocks of data, said transfer request comprising an address and a mask which indicates which of said sub-blocks are required as part of the request; (Column 1 lines 16-54). *The Examiner notes that the cache as a whole receives the transfer request as discussed supra with respect to claim 1,thus teaching the first interface.*
- generate a different address corresponding to each sub-block of said first block in response to receiving the transfer request; detect which of said sub-blocks are required as part of said transfer request; and utilize only those generated addresses which correspond to the sub-blocks which are required (Column1 lines 16-54) *The Examiner incorporates by reference herein the comments made supra with respect to claim 1.*

As per dependent claim **18**, Arimilli teach, detect which of said sub-blocks are required by examining said mask (Column 1 lines 16-54). *The Examiner notes that the "intra-cache line address", mask as shown supra, allows a particular byte to be selected, thus in order for the byte to be selected, the "intra-cache line address" must be examined.*

As per dependent claim **19**, Arimilli teach, wherein said mask comprises a plurality of bits, each of which correspond to a different sub-block of said first block, wherein a bit with a first value indicates said corresponding sub-block is required, and wherein a bit with a second value indicates said corresponding sub-block is not required (Column 1 lines 42-43 and 51-54). *The Examiner notes that the "intra-cache line*

address" as shown supra as the mask, allows a particular byte to be selected. The address itself is comprised of six bits, thus in order for the system to know which byte to select, the bits must indicate this. A particular byte being selected would require a particular bit to indicate this meaning the other bits indicate the other particular byte not being required.

As per dependent claim **20**, Arimilli teach, wherein said first interface is configured to generate each of said addresses corresponding to said sub-blocks concurrently (Column 1 lines 16-54).

As per dependent claim **21**, Arimilli teach, wherein said first interface is configured to detect which of said sub-blocks are required by: detecting a first bit of said mask which has a first value, wherein said first bit corresponds to a first sub-block; and selecting a first address of said generated addresses which corresponds to the first sub-block (Column 1 lines 16-54). *The Examiner notes that as discussed supra, the "intra-cache line address" corresponds to a 'first sub-block' and is selected based on its occupancy in the cache line.*

As per dependent claim **22**, Arimilli teach, wherein said first interface is further configured to: mask off said first bit of said mask, subsequent to utilizing said first address; detect a second bit of said mask which has a first value, wherein said second bit corresponds to a second sub-block; and select a second address of said generated addresses which corresponds to the second sub-block (Column 1 lines 16-54). *The Examiner notes that as discussed supra, the "intra-cache line address" allows the*

selection of a particular byte. The system requiring a different particular byte then as discussed supra makes the request indicating the other particular byte.

As per dependent claim **23**, Arimilli teach, wherein said first interface is further configured to: determine a first number of said sub-blocks are required; and detect transfer of all said required sub-blocks are complete, in response to detecting a number of sub-blocks equal to said first number have been transferred(Column1 lines 16-54). *The Examiner notes that as discussed supra, a particular byte is requested. Further, once the particular byte is selected, it is forwarded and thus the request is complete having transferred a single particular byte in response to the request for the particular byte.*

As per dependent claim **24**, Arimilli teach, wherein a number of sub-blocks required as part of the transfer request is equal to a sum of the number of bits which are asserted in the mask (Column 1 lines 16-54). *The Examiner notes that as taught and discussed supra, the "intra-cache line address" specifies which 'sub-block', "particular byte" will be selected. As shown in Arimilli, column 5 lines 40-67a logic 1 is used to identify requirements. Accordingly, a sum of all the bits in the "intra-cache line address" for a particular byte, 'sub-block' sums to a logic level 1 which is equal to the 1 particular byte, 'sub-block' that is required.*

As per dependent claim **25**, Arimilli teach, wherein a number of sub-blocks required as part of the transfer request is equal to a sum of the number of bits which are asserted in the mask (Column 1 lines 16-54). *The Examiner notes that as taught and discussed supra, the "intra-cache line address" specifies which 'sub-block', "particular*

byte" will be selected. As shown in Arimilli, column 5 lines 40-67a logic 1 is used to identify requirements. Accordingly, a sum of all the bits in the "intra-cache line address" for a particular byte, 'sub-block' sums to a logic level 1 which is equal to the 1 particular byte, 'sub-block' that is required..

As per dependent claim **26**, Arimilli teach, wherein a number of sub-blocks required as part of the transfer request is equal to a sum of the number of bits which are asserted in the mask (Column 1 lines 16-54). *The Examiner notes that as taught and discussed supra, the "intra-cache line address" specifies which 'sub-block', "particular byte" will be selected. As shown in Arimilli, column 5 lines 40-67a logic 1 is used to identify requirements. Accordingly, a sum of all the bits in the "intra-cache line address" for a particular byte, 'sub-block' sums to a logic level 1 which is equal to the 1 particular byte, 'sub-block' that is required.*

Response to Arguments

Applicant's arguments have been carefully and fully considered in light of the instant amendment filed 13 April 2006 and are persuasive. Therefore, the rejection has been withdrawn.

Any argument not specifically addressed is considered moot in light of the new ground(s) of rejection.

As noted supra in the response to amendment, this Office action is being issued in response to amendments to the claims made 18 November 2005. As such, this action has accordingly been made FINAL.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAS/mb

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